Claims

1. A method of resetting a jam latch comprising:

combining a respective data signal from each of a plurality of data lines to activate a first reset device;

activating a second reset device with a control signal; and

applying a reset voltage to a storage cell.

2. The method of claim 1, wherein combining the respective data signal from each of the plurality of data lines to activate the first reset device includes:

coupling the respective data signal from each of the plurality of data lines to an activation device; and

outputting an activation signal, from the activation device to the first reset device, when a level of the respective data signal from each of the plurality of data lines is substantially equal.

3. The method of claim 1, wherein the control signal includes a clock signal.

4. The method of claim 1, wherein the control signal is inverted.

5. The method of claim 1, further comprising disconnecting a voltage source from the storage cell.

6. The method of claim 5, wherein the voltage source is disconnected from the storage cell substantially simultaneously with activating the first reset device.

7. The method of claim 1, further comprising coupling a reset voltage across the activated first reset device and across the activated second reset device to apply the reset voltage to the storage cell.

8. The method of claim 1, wherein the plurality of data lines includes two or more data lines.

9. A jam latch reset circuit comprising:

an activation device having respective inputs coupled to each one of a plurality of data lines;

a first reset device having a first control input coupled to an output of the activation device, the first reset device having a reset voltage source coupled to an input of the first reset device;

a second reset device having a second control input coupled a control signal, the second reset device being coupled in series with the first reset device; and

a storage cell coupled to an output of the second reset device.

10. The circuit of claim 9, wherein an output of the storage cell is coupled to the output of the second reset device.

11. The circuit of claim 9, wherein the control signal is a timing signal.

12. The circuit of claim 9, wherein the activation device is a logic device.

13. The circuit of claim 9, wherein the activation device is a nand gate.

14. The circuit of claim 9, further comprising a voltage source coupled to the output of the storage cell through a voltage source controller.

15. The circuit of claim 14, wherein the voltage source controller includes a control input coupled to the output of the activation device.

16. The circuit of claim 14, wherein each of the voltage source controller, the first reset device, and the second reset device include transistors.

17. The circuit of claim 9, wherein the plurality of data lines includes two or more data lines.

18. The circuit of claim 9, wherein the storage cell includes a storage cell input and a storage cell output, the storage cell input being opposite the storage cell output, the output of the second reset device being coupled to the storage cell output, and an input circuit being coupled to the storage cell input.

19. A method of capturing data in a jam latch circuit comprising:

receiving a respective data signal on at least one of a plurality of data lines;

charging a storage cell on storage cell input;

outputting a data signal from a storage cell output;

combining the respective data signal from each of the plurality of data lines and the data signal from the storage cell output;

outputting a jam latch output data signal; and

resetting a jam latch circuit including:

combining the respective data signal from each of the plurality of data lines to activate a first reset device;

activating a second reset device with a control signal; and

applying a reset voltage to the storage cell.

20. The method of claim 19, wherein combining the respective data signal from each of the plurality of data lines to activate the first reset device includes:

coupling the respective data signal from each of the plurality of data lines to an activation device; and

outputting an activation signal, from the activation device to the first reset device, when a level of the respective data signal from each of the plurality of data lines is substantially equal.